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(Not for submission under 37 CFR 1.99)

Application Number	10544894
Filing Date	2006-07-19
First Named Inventor	Dasu, Aravind R.
Art Unit	2193
Examiner Name	Bullock Jr. Lewis Alexander
Attorney Docket Number	117316-155055

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1	Search Report, mailed 03/17/05 for application PCT/US04/03609	<input type="checkbox"/>
2	Abdulrahim, Mohammad A. " Parallel Algorithms for Labeled Graph Matching" PhD thesis Colorado School of Mines, 1998	<input type="checkbox"/>
3	Agarwal, A. et al. "The Raw Compiler Project" Proc of the Second SUIF compiler workshop, Stanford, CA, August 21-23, 1997	<input type="checkbox"/>
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7	Ammons, G., et al. " Exploiting Hardware Performance Counters with Flow and Context Sensitive Profiling" PLDI, June 1997	<input type="checkbox"/>
8	Arnold, M., et al. " Automatic Detection of Recurring Operation Patterns" Seventh International Workshop on Hardware/Software Co-Design (CODES'99), Rome Italy, May 1999	<input type="checkbox"/>
9	Arnold, M., et al. " Instruction Set Synthesis Using Operation Pattern Detection" Fifth Annual Conf. of ASCI, Heijen, The Netherlands, June 1999	<input type="checkbox"/>
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11	Athanasi, P. "A Functional Reconfigurable Architecture and Compiler for Adaptive Computing" Technical Report LEMS-100, Brown University, Division of Engineering, 1992	<input type="checkbox"/>

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12	Athanass, P., et al. "An Adaptive Hardware Machine Architecture and Compiler for Dynamic Processor Reconfiguration" International Conference on Computer Design, 1991	<input type="checkbox"/>
13	Ball, T., et al. "Efficient Path Profiling", Proceedings of MICRO-29, December 2-4, 1996, Paris, France	<input type="checkbox"/>
14	Basin, D.A., et al. "A Term Equality Problem Equivalent to Graph Isomorphism" Information Processing Letters, 54: 61-66, 1994	<input type="checkbox"/>
15	Becker, J., et al. "A Parallel Dynamically Reconfigurable Architecture Designed for Flexible Application-Tailored Hardware/Software Systems in Future Mobile Communication" The Journal of Supercomputing, 19 (1), 102-127, 2001	<input type="checkbox"/>
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17	Betz, V., et al. "VPR: A New Packing, Placement and Routing Tool for FPGA Research" International Workshop on Field-Programmable Logic and Application, pp. 213-222, 1997	<input type="checkbox"/>
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20	Bozorgzadeh, E., et al. "Rpack: Routability-Driven packing for cluster-based FPGAs" Proceedings of the Conference on Asia South Pacific Design Automation Conference, p. 629-634, January 2001, Japan	<input type="checkbox"/>
21	BRASS Research Group, Berkeley Reconfigurable Architectures, Systems, & Software, http://brass.cs.berkeley.edu	<input type="checkbox"/>
22	Brisk, P. et al. " Instruction Generation and Regularity Extraction For Reconfigurable Processors", International Compilers, Architecture and Synthesis for Embedded Systems (CASES), Pages 1-8, October 2002	<input type="checkbox"/>

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23	Brisk, P., et al. "Area-Efficient Instruction Set Synthesis for Reconfigurable System-on-Chip Designs" ACM DAC 2004, pages 395-400 (2004)	<input type="checkbox"/>
24	Brown, Fon R. III "Real-Time Scheduling with Fuzzy Systems, PhD thesis, Utah State University, 1998	<input type="checkbox"/>
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27	Cambouropoulos, Emilios "Extracting Significant Patterns from Musical Strings: Some Interesting Problems." London String Days 2000 Workshop, King's College London	<input type="checkbox"/>
28	Campi, F., et al. "A Reconfigurable Processor Architecture and Software Development Environment for Embedded Systems" International Parallel and Distributed Processing Symposium, 2003	<input type="checkbox"/>
29	Chameleon Systems Inc.- www.chameleonsystems.com, "Advanced Communications Technologies- Development Partnership with Chameleon Systems", Business Wire, December 26, 2000	<input type="checkbox"/>
30	Chekuri, C., et al. "Profile-Driven Instruction Level Parallel Scheduling with Application to Super Blocks" Proc of the 29th Annual International Symposium on Microarchitecture (MICRO-29) December, 1996	<input type="checkbox"/>
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32	Chen, D., et al. "A Reconfigurable Multiprocessor IC for Rapid Prototyping of Algorithmic-Specific High-Speed DSP Data Paths" IEEE Journal of Solid-State Circuits, 1992	<input type="checkbox"/>
33	Chou, P., et al. "Interval Scheduling: Fine-Grained Code Scheduling for Embedded Systems" Proc. ACM/IEEE DAC, 1995, 462-467	<input type="checkbox"/>

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34	Chowdhary, A. "A General Approach for Regularity Extraction in Datapath Circuits", Proc. Of International Conference on Computer-Aided Design, 1998	<input type="checkbox"/>
35	Chu, M. et al. "Object Oriented Circuit-Generators in Java", IEEE Symposium on FPGAs for Custom Computing Machines, April 1998.	<input type="checkbox"/>
36	Coffman, E., et al. " Optimal Scheduling for Two-Processor Systems" Acta Informatica, 1, 1972, 200-213	<input type="checkbox"/>
37	Cook, D., et al. " Knowledge Discovery from Structural Data" Journal of Intelligent Information Systems, 1995	<input type="checkbox"/>
38	Dasu, A., et al. " An Analysis Tool Set for Reconfigurable Media Processing" The International Conference on Engineering of Reconfigurable Systems and Algorithms, Las Vegas, June 2003	<input type="checkbox"/>
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41	De, V., et al. " A Heuristic Global Router for Polycell Layout" PhD thesis, Duke University, 1986	<input type="checkbox"/>
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43	Dehnert, J., et al. " Compiling for the Cydra-5," Journal of Supercomputing, 7: 181-228 (1993)	<input type="checkbox"/>
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45	Dehon, Andre. "The Density Advantage of Configurable Computing" Computer, vol. 33, no. 4, April 2000, pp. 41-49	<input type="checkbox"/>
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49	Fisher, Joseph A. " Global Code Generation For Instruction-Level Parallelism: Trace Scheduling-2" Tech. Rep. HPL 93-43, Hewlett Packard Labs, June, 1993	<input type="checkbox"/>
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